REMARKS/ARGUMENTS

In an Office Action dated April 20, 2006 claims 1,10, 19 and 28 were provisionally rejected under obviousness-type double patenting and claims 1-36 were rejected under § 103 over Edsall and Testardi. Applicants respectfully traverse the § 103rejections and request consideration of the following arguments.

Obviousness-type Double Patenting

Applicants submit a terminal disclaimer to overcome the obviousness-type double patenting rejection. Withdrawal is requested.

§ 103 Rejections

Applicants respectfully submit that the present claims are allowable.

Claim 19

Claim 19 is being treated as an exemplary claim in these remarks to better track the Office Action. The Office Action rejected claim 19 over Edsall and Testardi. The Office Action equates the claimed control module to be the fast paths and control paths of Testardi and then states that the control module is configured to perform data migration. However, the claim language is "said input/output module and said control module being configured to interactively perform data migration . . ." Thus the Office Action has omitted the requirement that the input/output module and the control module interactively perform data migration, indicating only that Testardi shows the control module equivalent performs data migration, with no reference to the input/output module or interactivity between the two modules.

Because this required element of claim 19, and similar claims 1, 10 and 28, is missing, Applicants submit that all of the present claims are allowable.

Claim 21

As an exemplary claim, Applicants will address the rejection of claim 21. The Office Action stated that Testardi disclosed the processors delaying data write operations if said barrier entry relates to said data write operation by referencing paragraph 207 in Testardi.

Applicants respectfully submit this mischaracterizes the relevant portion of Testardi. Quoting Testardi from paragraph 207:

> Only a write operation being performed to the copy barrier range itself is actually faulted to the CP to be later retried once the copy barrier range moves to the subsequent extent of the Rmap.

The claim defines the processors as being located in the input/output module. The rejection is based on Testardi control path operation, previously defined in the Office Action as being in the control module. Operation of the preferred embodiment of the present application is described in paragraph 222 of the published application. Faulting the CP of Testardi is an inefficient and slow process as opposed to the simple delay by the processors of the claimed invention, which processors are receiving, operating on and transmitting the network traffic in the input/output module. There is no teaching or suggestion to transfer handling this case, and doing a delay rather than a fault, to the processors in the input/output module.

Applicants submit that claim 21 and similar claims 3, 8, 12, 17, 26, 30 and 35 are allowable.

CONCLUSION

Based on the above remarks Applicants respectfully submit that all of the present claims are allowable. Reconsideration is respectfully requested.

Respectfully submitted,

July 19, 2006

Filed Electronically

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